REMARKS

Claims 1, 4, 6, 7, 11-13, and 16-19 have been amended. Claims 1-19 are currently pending in the case. Further examination and reconsideration of the presently claimed application is hereby respectfully requested.

Section 112 Rejection

Claim 4 was rejected under 35 U.S.C § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. To expedite prosecution, claim 4 has been amended for clarification purposes. As such, claim 4 does not present new subject matter. This amendment is believed to clarify the claim language in a manner that addresses the concerns expressed in the Office Action. Accordingly, removal of the § 112, second paragraph, rejection of claim 4 is respectively requested.

Section 102 Rejection

Claims 1-5, 7-11, 13, and 16-19 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,929,664 to Alleven (hereinafter "Alleven"). The standard for "anticipation" is one of fairly strict identity. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987), MPEP § 2131. The cited art does not disclose all limitations of the currently pending claims, some distinctive limitations of which are set forth in more detail below.

Alleven does not teach or suggest a circuit comprising a comparator having an output and a pair of inputs, and a pull-up transistor coupled between a power supply and one of the pair of inputs. Amended independent claim 1 recites:

> A circuit, comprising a comparator having an output and a pair of inputs, wherein the pair of inputs are adapted to receive an output signal produced from the circuit and a reference voltage forwarded to the circuit, and wherein the circuit further comprises ... a pull-up transistor coupled between a power supply and said one pair of inputs.

Support for the amendments to claim 1 may be found in the Specification, for example, on page 8, lines 13-14 and in Fig. 3.

Alleven discloses a method to improve crossover performance and/or monotonicity for a universal serial bus low-speed output driver. (Alleven -- Title). Alleven, however, does not teach or suggest a circuit comprising a comparator having an output and a pair of inputs and a pull-up transistor coupled between a power supply and one of the pair of inputs. In fact, under the section of Allowable Subject Matter, the Office Action admittedly states, "none of the prior art teaches or fairly suggests 'a pull up transistor' limitation as required in claim 6." (Office Action -- page 4 - page 5). As shown above, claim 1 has been amended to include the limitation of a pull-up transistor, as described in claim 6. Therefore, Alleven does not teach or suggest all limitations of claim 1.

Alleven also does teach or suggest a pull-down transistor coupled to an output of a comparator for fixing a minimum voltage of an output signal to a voltage approximately equal to the reference voltage whereby the pulse width of the output signal varies in proportion to changes in the reference voltage. Amended independent claim 7 recites in part: "a comparator coupled to compare a voltage of the output signal to the reference voltage; and a pull-down transistor coupled in combination with the comparator for fixing a minimum voltage of the output signal to a voltage approximately equal to the reference voltage whereby the pulse width of the output signal varies in proportion to changes in the reference voltage." Support for the amendments to claim 7 may be found in the Specification, for example, on page 9, lines 19-21.

Alleven discloses a method to reduce output buffer delays. (Alleven -- column 2, lines 31-32). Alleven, however, does not teach or suggest a pull-down transistor coupled to an output of a comparator for fixing a minimum voltage of an output signal to a voltage approximately equal to the reference voltage whereby the pulse width of the output signal varies in proportion to changes in the reference voltage. Alleven discloses, "[t]he reference voltage in Fig. 3 is generally configured to be a threshold voltage. By varying the threshold voltage, the particular amount of delay introduced by the delay circuit 36 may be adjusted." (Alleven -- column 4, lines 61-64). As such, Alleven discloses for each reference voltage value, there is an associated time delay. For example, Alleven discloses "if the voltage reference Vref is set at the voltage threshold (e.g. Vthreshold1), the delay from the delay circuit generally corresponds to a first time delay (e.g., tD1), illustrated in the time axis t of the diagram [Fig. 6]. If the voltage reference signal reference is decreased to equal the threshold voltage Vthreshold2, the delay presented from delay circuit 36 may be equal to a time delay (e.g., tD2)." (Alleven -- page 4, line 66 through page 5, line 5). As such, Alleven merely discloses a means to adjust a reference voltage to thereby alter a time delay. Such a means, however, cannot be construed to teach or suggest a means (such as a pull-down transistor and a

comparator) for fixing a minimum voltage of an output signal to a voltage approximately equal to the reference voltage whereby the pulse width of the output signal varies in proportion to changes in the reference voltage. Thus, Alleven does not teach or suggest all limitations of claim 7.

Alleven does not teach or suggest a pull-down transistor adapted to chop an output signal between a periodic and symmetric positive peak voltage value and a reference voltage. Independent claim 16 recites in part: "a method for regulating a duty cycle of an output signal, comprising ... a comparator for comparing the output signal to a predetermined reference voltage and feeding back the results of the comparison to a pull-down transistor that chops the output signal between a periodic and symmetric positive peak voltage value and the reference voltage."

Alleven discloses a method and circuit that compensates for voltage spikes at the output. (Alleven -- column 2, line 32). However, Alleven does not teach or suggest a pull-down transistor adapted to chop an output signal between a periodic and symmetric positive peak voltage value and the reference voltage. In particular, Alleven discloses current source 244, resistor 218, and transistors N1, N2, and P1 of Figure 9. Resistor 218 and transistors N1, N2, and P1 "may be coupled together to provide the D- output." (Alleven -- column 5, lines 52-53). Alleven discloses current source 244 "compensates for the effect of the pull-up resistor" until it is turned off. (Alleven -- column 5, lines 67 through column 6, lines 4). Such an "effect" is an overshoot of the D- output (see Fig. 10) and is described by Alleven as "bump 262 [which] results from the presence of resistor 218." (Alleven -- column 6, lines 11-12). After current source 244 is turned off, the D- output "may then operate as a function of only transistor N1 (and the transistor P1)." (Alleven -- column 6, lines 4-5). In this manner, Alleven illustrates how compensatory effects of current source 244 enables bump 262 to be reduced and/or eliminated. Alleven, however, does not illustrate in any of the waveforms of Figs. 10-12 that the D- output signal could be chopped between periodic and symmetric positive peak voltage value and a reference value. Instead, Alleven clearly illustrates the D- output signal as transitioning between positive peak to a negative peak with or without the compensation from current source 244 or transistor N1. Consequently, Alleven does not teach or suggest all limitations of claim 16.

For at least the aforementioned reasons, claims 1, 7, and 16 are not anticipated by the cited art. Therefore, claims 1, 7, and 16, and claims dependent therefrom, are patentably distinct over the cited art. Accordingly, removal of the § 102(b) rejection of claims 1-5, 7-11, 13, and 16-19 is respectfully requested.

Section 103 Rejection

Claim 15, which is dependent from claim 7, was rejected under 35 U.S.C. § 103(a) as being unpatentable over Alleven. As noted in the above, Alleven does not teach or suggest all limitations of independent claim 7. Therefore, independent claim 7, as well as claims dependent therefrom, are patentably distinct over the cited art. Accordingly, removal of the § 103(b) rejection of claim 15 is respectfully requested.

Allowance of Claims

Claims 6, 12, and 14 were objected to as being dependent upon rejected base claims, but would be deemed allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant sincerely appreciates the Examiner's recognition of the patentable subject matter recited in these claims. However, as set forth above, claims 1 and 7, as well as claims dependent therefrom, are patentably distinct over the cited art. Accordingly, removal of the objection to claims 6, 12, and 14 is respectfully requested.

CONCLUSION

This response constitutes a complete response to all issues raised in the Office Action mailed November 15, 2002. In view of the remarks traversing rejections, Applicants assert that pending claims 1-19 are in condition for allowance. If the Examiner has any questions, comments, or suggestions, the undersigned attorney earnestly requests a telephone conference.

No fees are required for filing this amendment; however, the Commissioner is authorized to charge any additional fees which may be required, or credit any overpayment, to Conley Rose, P.C. Deposit Account No. 03-2769/5298-07400.

Respectfully submitted,

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ATTACHMENT A
"Marked-Up" Amendments

IN THE CLAIMS

Please amend claims 1, 4, 6, 7, 11-13, and 16-19 as follows. Also following is list of the pending claims.

1. (Amended) A circuit, comprising a comparator having an output and a pair of inputs, wherein the pair of inputs are adapted to receive an output signal produced from the circuit and a reference voltage forwarded to the circuit, and wherein [the output is coupled to] the circuit further comprises:

a pull-down transistor [that is] connected to one of the pair of inputs and the output; and

a pull-up transistor coupled between a power supply and said one of the pair of inputs.

2. (Unchanged) The circuit as recited in claim 1, wherein said one of the pair of inputs is coupled to receive the output signal.

3. (Unchanged) The circuit as recited in claim 1, wherein the positive input of the pair of inputs is adapted to receive the output signal and the negative input of the pair of inputs is adapted to receive the reference voltage.

4. (Amended) The circuit as recited in claim 1, wherein the pull-down transistor comprises a gate conductor and a source-to-drain current path [formed]between said one of the pair of inputs and a ground supply voltage whenever a voltage of the output [signal] coupled to the gate conductor exceeds the reference voltage.

5. (Unchanged) The circuit as recited in claim 1, further comprising a current source coupled in parallel with the pull-down transistor between said one of the pair of inputs and a ground supply voltage.

6. (Amended) The circuit as recited in claim 1, [further comprising a] wherein the pull-up transistor [having] comprises a gate conductor and a source-to-drain current path [formed], which is operably coupled between [a] the power supply voltage and said one of the pair of inputs whenever a voltage of an

input signal coupled to the gate conductor exceeds a voltage of the output signal by a threshold voltage of the pull-up transistor.

7. (Amended) A system for adjusting [the] a pulse width of an output signal, comprising:

a circuit for maintaining a reference voltage between [the] positive and negative voltage peaks of the output signal; [and]

a comparator coupled to compare a voltage of the output signal to the reference voltage; and

a pull-down transistor coupled to an output of the comparator [and, depending in part on the slew rate and/or gain of the comparator,] for fixing [the] a minimum voltage of the output signal to a voltage approximately equal to the reference voltage whereby the pulse width of the output signal varies in proportion to changes in the reference voltage.

8. (Unchanged) The system as recited in claim 7, wherein the output signal comprises a duty cycle that varies in proportion to changes in the reference voltage.

9. (Unchanged) The system as recited in claim 7, wherein the circuit is adapted to increase the reference voltage and thereby cause a corresponding decrease in the pulse width and a duty cycle of the output signal.

10. (Unchanged) The system as recited in claim 7, wherein the circuit is adapted to decrease the reference voltage and thereby cause a corresponding increase in the pulse width and a duty cycle of the output signal.

11. (Amended) The system as recited in claim 7, wherein portions of the output signal below the reference voltage are chopped and remove at the reference voltage.

12. (Amended) The system as recited in claim 7, wherein the comparator comprises a [the] slew rate and/or gain [of the comparator], which is predetermined to preclude a voltage of the output signal from being less than the reference voltage.

13. (Amended) The system as recited in claim 7, [further comprising a] wherein the pull-down transistor [having] comprises a gate conductor and a source-to-drain current path, wherein the gate conductor is coupled to receive an output from the comparator and the source-to-drain current path is maintained during times when the reference voltage is maintained at approximately a midline voltage between the positive and negative voltage peaks of the output signal.

14. (Unchanged) The system as recited in claim 13, wherein the comparator comprises a predefined slew rate and/or gain so that an output voltage from the comparator will not go below a threshold voltage of the pull-down transistor.

15. (Unchanged) The system as recited in claim 7, further comprising an optical signal transmitter coupled to receive the output signal.

16. (Amended) A method for regulating a duty cycle of an output signal, comprising presenting the output signal into a comparator for comparing the output signal to a predetermined reference voltage and feeding back the results of the comparison to a pull-down transistor that chops the output signal between a periodic and symmetric positive peak voltage value and the reference voltage, whereby the time at which the positive peak voltage value extends above the reference voltage is directly proportional to the duty cycle of the output signal.

17. (Amended) The method as recited in claim 16, wherein said presenting comprises connecting a positive input of [a] the comparator to a conductor that receives the output signal and connecting a negative input of [a] the comparator to a conductor that receives the reference voltage.

18. (Amended) The method as recited in claim 16, wherein said feeding back comprises forwarding a voltage [that] which remains above a threshold voltage of [a] the pull-down transistor, from the comparator to a gate conductor of the pull-down transistor to ensure the pull-down transistor is always active.

19. (Amended) The method as recited in claim 16, wherein said feeding back comprises chopping a negative-going waveform of the output signal [to a steady state said] at a level of the reference voltage [that, if variable,], and wherein varying the level of the reference voltage changes the pulse width and duty cycle of the output signal.